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characteristic reduces the ratio of resistance of the "on" and "off" states of the transistor, often referred to as the on/off ratio. A large on/off ratio is desirable to support maximum circuit fanout (the number of transistor gates a transistor can drive with acceptable switching speed) and to provide maximum signal voltage swing close to the power supply voltage. Therefore, there is a trade-off between limitation of floating body effects and maintaining a suitable on/off ratio.

Page 4, line 6+:

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These approaches use angled implants which are asymmetrically placed due to shadowing by a (possibly dummy) gate structure and are largely characterized by substantial process complexity and diffusion of impurities over substantial distances which prevents the formation of sharp impurity concentration gradients and results in low precision of impurity structure placement. The proposed processes also do not provide for differences in impurity concentration between the source and drain but only differences in location. In summary, while some asymmetry is provided, the flexibility of design parameters in accordance with the proposed processes is very limited and, while source and drain characteristics may be made to differ somewhat, the diode characteristics cannot be accurately tailored or independently fabricated.

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In order to accomplish these and other objects of the invention, a method of forming an asymmetric field effect transistor to control floating body effect and a transistor having reduced or eliminated floating body effects formed by such a process is provided wherein the method or process includes steps of defining a gate location with a trench in a dielectric layer on a

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semiconductor layer, supplying impurities to the semiconductor layer at edges of the trench and adjacent source and drain regions, and forming a gate structure on the semiconductor layer in the trench. The impurities are supplied by angled implantation and/or diffusion from a doped solid body formed in the trench to accurately locate desired impurities such that diffusion is not required to drive the impurities to a desired location; thus supporting steep impurity concentration gradients and high performance.

In the claims:

Please substitute the following claims 12, 15 - 17 and 21 for the like-numbered claims as amended on January 8, 2003. A marked up copy of this claim showing the current changes is attached as an appendix to this amendment.

12. (Twice amended) An asymmetric field effect transistor comprising:

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a semiconductor layer, said semiconductor layer including impurities supplied thereto at edges of a trench in a dielectric layer on said semiconductor layer and adjacent source and drain regions, wherein the impurities have a location precisely defined by said edges of said trench to produce asymmetrical diode properties at said source and drain regions for reducing floating body effects, said semiconductor layer being formed on an insulator layer, and

a gate structure formed on said semiconductor layer in said trench.

15. (Twice Amended) a transistor as recited in claim 13, including a further insulator layer deposited over said source and drain regions and said gate structure.

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